REMARKS

(A) 35 USC 103 Rejections:

A 35 U.S.C. 103(a) rejection requires that all differences between the claimed design and sighted prior art reference(s) be identified in the rejection. As shown below, altering only a configuration memory circuit to a hard-wired circuit was neither identified nor considered inconsequential from a design viewpoint in the rejection stated. The applicant has further provided arguments to support that the invention could not be obvious to a person having "ordinary skill in the art" in view of the sighted prior art.

(A1) Disclosure summary:

Primary reference, Singh et al. (US 7,038,490) is related to an FPGA conversion to an ASIC (in Singh, term ASIC is synonyms with MPGA). Singh conversion fall into generic conversion described by Applicant on page 9 lines 9-21. There is a one-to-one LUT logic block match between FPGA and ASIC to map all logic. There is a corresponding routing structures between FPGA & ASIC to provide required interconnect. The FPGA has extra user configurable resources absent in the ASIC (ref. col 2 lines 54-58). The ASIC has extra timing tunable resources absent in the FPGA. FPGA signal propagation delay is "matched" to ASIC by adding programmable diode loads (ref. col 5 line 40) and programmable buffers delays (ref. col 5 line 60) to the ASIC device. These additions are identified by a software tool. The ASIC die size is smaller than the FPGA die size (ref. col 2 lines 3-5) which lowers ASIC manufacturing cost. In conclusion, Singh pertains to an FPGA to ASIC design conversion with similar LUT logic & different routing structure, where timing matching is handled by delay insertions.

Secondary reference Duong et al. (US 5,600,264) is related to a programmable 1-buffer, 6-transistor switch box to connect wires. The buffer provides the capacity to buffer a signal at the switch box if desired. Duong pertains to a specific switch box within a generic FPGA. There is no design conversion in Duong.

The Applicant discloses an FPGA to ASIC design conversion that comprises hard-wiring configuration memory circuits in the FPGA. Timing is guaranteed to be identical in both as they both have the identical base-die (all transistors, wires, etc.). In contrast to Singh, both FPGA and ASIC devices have identical die size, and no timing tunable structures are added (or deleted) to meet exact timing. The cost reduction is achieved by improved yield resulting from higher redundancy in the ASIC. In contrast to Duong, the Applicant discloses a convertible FPGA

independent of specific programmable elements as opposed to a novel programmable switch-box element. The Applicant will provide detailed analysis of these differences to traverse the examiner's rejection.

(A2) Detailed analysis:

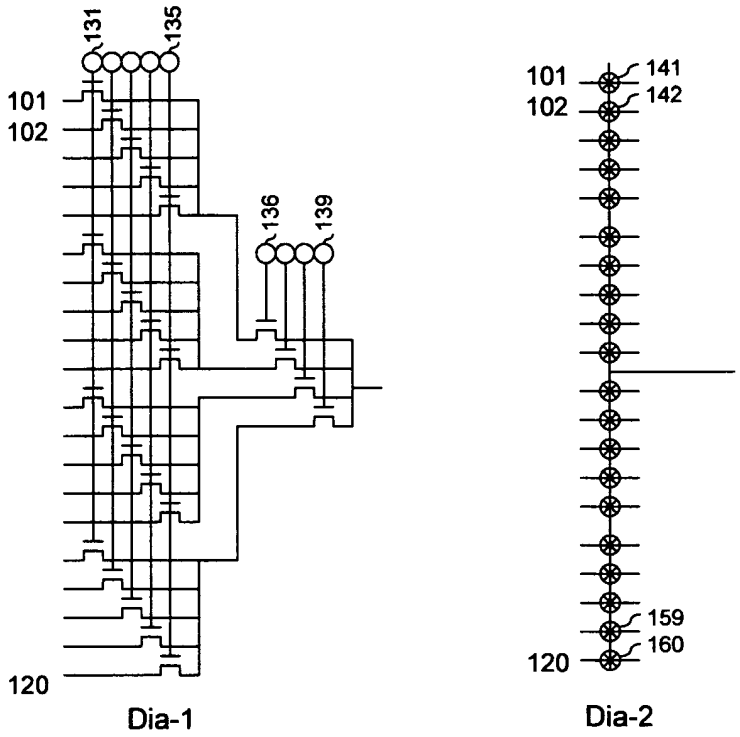
(A2-1) IC (PFU logic) die size: In Singh, Fig-1 and Fig-2 compares an FPGA 100 and ASIC 200 that are claimed to have similar timing. PFU/LUT structure for Fig-2 is shown in Fig-3. In the PFU structure for Fig-1 LUT inputs are held in SRAM, while in PFU structure for Fig-3 LUT inputs are held by Vcc/Vss wire coupling. Hard-wiring LUT structures were demonstrated by the Applicant in related incorporated by reference Application Serial Numbers 10/267,483 and 10/267,511 (now US 6,747,478) both filed 10/08/2002 predating Singh disclosure. In Singh, assume CMOS construction of Fig-3 circuit (Applicant's has shown an NMOS LUT circuit in Fig-8B). 2-input CMOS MUXs 310 & 320 comprises 12 transistors (6 NMOS and 6 PMOS) each. 1-input MUX 330 comprises 4 transistors. 2-input XOR2 360 comprises 12 transistors. The entire ASIC LUT circuit in Fig-3 comprises 76 transistors. The FPGA LUT circuit requires Fig-3 circuit + 16 extra SRAM bits, each SRAM bit comprising 6 transistors; a total of 96 extra transistors compared to ASIC. PFU-00 for FPGA (Fig-1) has 172 transistors. PFU-00 for ASIC (Fig-2) has 76 transistors. The ratio between the two is 2.26. Therefore the X-dimension (row length) and Y-dimension (column height) for Fig-1 FPGA is larger than Fig-2 ASIC. Any wire length such as 20 in X or Y dimension is much shorter in Fig-2 compared to Fig-1. They may span the same number of PFUs in X & Y directions, but the length is much shorter for the ASIC. This is important as the wire signal propagation delay depends on "RC" component of a wire, which scales as L^2 for wire length L (ref App-2). A simplistic view of identical rows and columns between FPGA and ASIC is NOT a sufficient criterion to match the distance L between two nodes or the signal timing delay between the two nodes.

(A2-2) IC (routing) die size: Pages 1-4 of Xilinx Inc. (a leading FPGA vendor) product specification for "Platform Flash ISP Configuration PROMs" DS-123 (v2.9) May 09, 2006 is enclosed as Appendix-1. The number of configuration bits for Xilinx FPGA products is shown on pages 3 & 4. For example, on page 3, Virtex-II Pro FPGA's comprise 1,305,376 – 34,292,768 configuration bits. Specifically mid-density XC2VP7 device comprises 4,485,408 configuration bits; of which 3,674,400 bits program the FPGA and 811,008 are for Dual-Port 44x18K user

memory (extracted from data sheets). Of the 3,674,400 SRAM bits, LUTs (in logic PFUs) take up 296,960 bits (extracted from data sheets) while remaining 3,377,440 bits program other features (mostly wire MUXs). In short, in Singh Fig-1, only ~ 8% of SRAM are in PFUs, while majority 90+% SRAM supports wires in interconnect structure. A two stage 20:1 NMOS MUX (such as MUX 505 in Singh Fig-2) requires 24 NMOS transistors and 9 SRAM (54 transistors) bits for the FPGA version (see Dia-1) and zero transistors for the via-MUX ASIC version (see Dia-2, and known as a crossbar). The transistor ratio between the FPGA and ASIC is infinite (very different from PFU area ratio). It is customary to use 2-stage NMOS MUXing for FPGA routing as Singh is silent on MUX construction. It is easily seen that without crossbar transistors in the ASIC, routing area is significantly smaller for the ASIC. One familiar in design of FPGA & ASIC knows that MUXs are inter-dispersed between PFUs of Fig-1 FPGA, and crossbars are overlaid on top of PFUs of Fig-2 ASIC. The different area reduction ratios between MUX & PFU regions make the wire length reductions non-uniform and unpredictable between retained logic transistors between FPGA and ASIC. This is also important as the wire signal propagation delay which depends on "RC" component of a wire (scaling as L^2 for wire length L) is unpredictable and non-linear between Singh FPGA and Singh ASIC. The wire delays are further exacerbated by the neighboring wires as well. It is not possible to fit the same number of wires within FPGA 100 into ASIC 200 as the die area has reduced drastically. Even changing power/ground neighboring wires affect signal transit time due to shielding effects caused by the power/ground bus lines.

(A2-3) IC performance: In Singh, Fig-5 & Fig-6 depicts two signal paths proposed to have identical timing between FPGA of Fig-1 and ASIC of Fig-2. This is one path out of billions of similar other paths between the FPGA and ASIC. For identical timing, clearly all billions of these paths must provide substantially identical timing between the FPGA and ASIC. Singh acknowledges that ASIC die size is smaller than the FPGA die size (ref. col 2 lines 3-5). Sections A2-1 & A2-2 describe fundamental reasons for the area difference while further illustrating the wire length and timing differences ensuing from such area difference. One of ordinary skill will construct a 20:1 2-stage MUX structure (505 in Fig-5) as shown in Dia-1, and a 20:1 via MUX structure (605 in Fig-6) as shown in Dia-2 (also known as a crossbar). The via MUX construction shown in Dia-2 is supported by Singh in col 5 line 13: "*Referring again to Fig-6, depending upon which multiplexer 505 is programmed to select for, the same signal in ASIC 200*

is connected by via 605 to routing structure portion 600". Further please see col 5 lines 23-46 wherein diodes are inserted to ASIC to compensate for missing NMOS diffusion capacitance in



ASIC 200. In Dia-1 (FPGA) one input wire from 20 wires 101-120 can be selected by programming 9 SRAM bits 131-139. The signal passes through two ON state NMOS devices, incurring related gate delays. In Dia-2 (ASIC) the same input wire can be selected by inserting a via at the right location of 20 available via sites 141-160. There is no gate delay for signal transfer. The signal transit time through the switch in Dia-1 is well known to be much slower than that in Dia-2 due to these NMOS gate delays. The signal level in Dia-1 is well known to be "NMOS threshold-voltage" lower at the output of the switch compared to that in Dia-2. Both these alter buffer 505 trip point compared to buffer 615 trip point. In addition, the loading seen by drivers generating MUX input signals are also substantially lower for the ASIC. Singh attempts to adjust for some of these timing variances by inserting two new "discrete step delay" structures into the ASIC 200 compared to FPGA 100. These two discrete components comprise: (i) programmable diode loads (ref. col 5 line 40) to adjust for MUX loads, and (ii) programmable buffers delays (ref. col 5 line 60) to adjust for wire delays. The very same techniques are common in the ASIC industry to generate a "continuum of delays" in trying to match signal timing during PLD to ASIC design conversions. However, as Singh him-self states in col 1 line

32: "*For example, although the ASIC will implement the same logic programmed into PLD, the propagation delays for various signals within the ASIC will differ from the same delays encountered in the PLD*". Clearly the Singh ASIC has the very same problem as interconnect delays are grossly different between the FPGA 100 and ASIC 200 in spite of maintaining similar logic PFU/LUT structures.

(A2-4) IC interconnect: In Dia-1 and Dia-2, Singh 20:1 MUX structures in Fig-5 and 20:1 crossbar in Fig-6 are shown. The interconnect structure to support these two structures are vastly different as detailed in this section. In Dia-1, inputs 101-120 represent 20 metal wires that may be in a number of available metal layers such as metal-1 (390 in Fig-4a), metal-2 (385 in Fig-4a) etc. In FPGA's at 90nm process technology, 9 metal layers are available to fit all the interconnect wires that are required. In Appendix-2 "Automated conversion from a LUT-based FPGA to LUT-based MPGA with fast turnaround time", Veredeas et al., pp 36-41, EDAA, 2006 is provided for the Examiner's perusal. In that, under sec 2.1 it is specifically stated that Xilinx Virtex-II Pro device family utilizes 9 layers of metal. In sec 2.2 line 10 it is stated that FPGA LUT element is retained in MPGA with Vdd/Vss connections (same as Singh ASIC). In Fig-1 and sec 2.2 line 14 it is shown that logic in MPGA is identical to that to Virtex FPGA (same as with Singh). In Fig-2 the MPGA tile with metal wire crossbar (via MUX) is presented which is same as 605 in Fig-6 of Singh. The conversion difficulty is presented in sec 3, and in 1st line of 2nd column on page 38 it is stated that: "*the logic delays are assumed equal. The delay difference is in the interconnect*". The conversion goal (page 38 sec 3 line 1) is to keep timing similar or better in the MPGA compared to FPGA. In sec 3.2 it is presented (line 2) that wire delay is quadratic to wire length, and Fig-4 shows an equivalent RC network for interconnect delay. Under sec 4, experimental results are presented for design conversions, and specifically Tab-4 tabulates the signal delays between Virtex FPGA and two cases of MPGA – one without buffer insertions and one with buffer insertions. As can be seen neither of these have substantially identical timing between the FPGA and the MPGA. The last para on page 40 (under sec 4) states that 1%-2% of nets had longer delays than the FPGA, and it is understood that 98%-99% of nets had shorter delays than the FPGA. This article is an independent finding of what is commonly known in the art of converting designs. Singh ASIC is a completely different IC design from original Singh FPGA, just as Veredas Zelix is a completely different MPGA design from original Xilinx Virtex FPGA. Singh design conversion falls into conventional conversions.

(A2-5) IC design: It has been shown that two key active-area components (i.e. transistor level layout geometries) are absent between FPGA 100 (Fig-1) and ASIC 200 (Fig-2) of Singh. Those are: (i) Millions of SRAM bits that hold configuration data in FPGA, and (ii) Millions of NMOS transistors that are needed for MUXs in FPGA. It is further demonstrated that two added active-area components are inserted into ASIC 200 that were not present in FPGA 100. Those are: (i) millions of programmable diodes, and (ii) millions of programmable buffers. This order of magnitude transistor change requires modifying every single mask between the FPGA and ASIC. It is further shown that the ASIC has to be completely re-engineered to construct a completely new wire interconnect structure comprising crossbar switches to map the original MUX switches within FPGA. It is absolutely clear that not even one mask can be identical between the two Singh ICs.

The Applicant respectfully submits that two separate devices comprising different active area geometries, metal wires and different die sizes do not posses identical or similar timing by simply stating so in the disclosure. Every single mask in Singh is different between FPGA and ASIC. The timing between two devices can be only exactly matched if the two devices have identical layouts between two canonicals as presented in Applicant's current disclosure. This is a necessary condition for timing exactness. Timing exact canonicals wherein every timing path is exactly the same between the two canonicals is a fundamental difference between Singh in view of Duong over the Applicant's disclosure, and a basis to traverse the examiner's rejection. One or more masking patterns invariant to memory construction is another fundamental difference between Singh in view of Duong over the Applicant's disclosure, and a basis to traverse the examiner's rejection.

(A3) Applicant's independent claim elements:

(A3-1) Claim-1: Applicant's claim 1 recites:

> 1. An integrated circuit (IC) comprising:
> a first selectable fabrication option comprised of a user configurable memory circuit; and
> a second selectable fabrication option comprised of a hard-wired circuit in lieu of said user configurable memory circuit;
> wherein, the IC functionality and performance is substantially identical for a given configuration utilizing the first or second fabrication options.

A) Singh (in view of Duong) fails to show "*a second selectable fabrication option comprised of a hard-wired circuit in lieu of said user configurable memory circuit*". The wire structure of Singh device is completely hard-wired and does not replace a configurable memory circuit of an FPGA. The Applicant defines configuration circuits on page 16 line 6 as follows:

> "The term configuration circuit includes one or more configurable elements and connections that can be programmed for controlling one or more circuit blocks in accordance with a predetermined user-desired functionality. The configuration circuit includes the memory element and the access circuitry, herewith called memory circuitry, to modify said memory element. Configuration circuit does not include the logic pass-gate controlled by said memory element".

In Singh Fig-5, MUX 505 comprises: (i) configuration memory circuit (not shown, but similar to Applicant's 350 in Fig-3a & bubbles 131-139 in Dia-1), and (ii) logic circuits (wires X6, X2, X1, F/Q and NMOS transistors within MUX 505). SRAM elements in configuration memory circuits can be programmed to control MUX 505. In constructing crossbar 605 for the ASIC, all configuration circuits and logic circuits (NMOS inside MUX 505) are replaced by new hard-wire interconnect. In contrast, in Applicant's Fig-3B and Fig-6, it is clearly shown that only configuration memory circuit 350 is replaced by a hard-wired circuit without affecting the logic circuit (NMOS 310 & 610 respectively). Modifications to logic circuits affect signal delays, and not doing so is a salient feature of the Applicant's invention. Duong provides no added value.

B) Singh fails to demonstrate "*IC functionality and performance is substantially identical for a given configuration utilizing the first or second fabrication options*". This has been presented by Applicant in Sec A2 above, and further independently verified by reference provided in Appendix-2. When every signal path is altered, any assertion on timing equivalence is invalid. These differences are added bases to traverse the examiner's rejection.

(A3-2) Claim-8: Applicant's claim 8 recites:

> 8. A programmable logic device (PLD) comprising:
> two selectable memory construction options to control logic circuits, wherein:
> a first selectable option comprises a random access memory (RAM) construction; and
> a second selectable option comprises a hard-wire read only memory (ROM) construction;
> wherein, the logic circuits construction comprises one or more masking patterns that are invariant to the memory construction options.

A) Singh fails to show "*a second selectable option comprises a hard-wire read only memory (ROM) construction*". The crossbar structure of Singh device is a fully hard-wired circuit and does not comprise a read only memory element. It requires metal layers and via connections to complete wire interconnects, similar to all gate-arrays. This is further detailed in Sec A4-2.

B) Singh fails to show "*the logic circuits construction comprises one or more masking patterns that are invariant to the memory construction options*". In Singh, every single mask is different between FPGA 100 and ASIC 200. This has been presented in detail under Sec A2.

These differences are added bases to traverse the examiner's rejection.

(A3-3) Claim-17: Applicant's claim 1 recites:

> 17. A configurable pass-gate logic element to electrically couple two nodes in a programmable logic device (PLD), comprising:
> a configuration circuit to configure the pass-gate logic element, said configuration achieved by a memory element in the configuration circuit, wherein the memory element construction comprises:
> a first selectable option comprising a random access memory (RAM) construction; and
> a second selectable option comprising a hard-wire read only memory (ROM) construction;
> wherein, the pass-gate logic element construction comprises one or more masking patterns that are invariant to the memory construction options.

A) Singh fails to show "*A configurable pass-gate logic element ... said configuration achieved by a memory element ... wherein the memory element construction comprises a second selectable option comprising a hard-wire read only memory (ROM) construction*". The wire structure of Singh second device is completely hard-wired. There is no pass-gate in this option. Furthermore there is no read only memory construction in the second option. It requires only metal layers and via connections to complete wire interconnects.

B) Singh fails to show "*the pass-gate logic element construction comprises one or more masking patterns that are invariant to the memory construction options*". In Singh, every single mask is different between FPGA 100 and ASIC 200. This has been presented in Sec A2 above.

These differences are added bases to traverse the examiner's rejection.

(A4) Examiner's rejection criteria:

(A4-1) Claim-1: On page-2 of the office action, in rejecting claim-1, the examiner stated that:

> *"a first selectable option comprising (FPGA 5 in Fig-1 and circuit shown in Fig-5) comprised of a user configurable circuit (multiplexer 505; col 4, lines 50+): and a second selectable fabrication option (ASIC in Fig-2 and circuit shown in Fig-6) comprised of a hard-wired circuit in lieu of said user configurable circuit (col 5, lines 3-57), wherein, the IC functionality and performance is substantially identical for a given configuration utilizing the first or second fabrication options (col 5, lines 3-57)".*

The Applicant's claim-1 is specific to configurable memory circuit fabrication options. It does not pertain to configurable circuit as the examiner sited in the rejection. Every FPGA design converted to an ASIC/Gate Array design replaces user configurable circuits by hard-wired circuits. Such conversions do not replace user configurable memory circuits by hard-wired circuits between two options. This is novel and presented by the Applicant. Multiplexer 505 is not a configurable memory circuit (Applicant's definition on page 16 line 6+) as it comprises logic elements such as NMOS gates shown in Dia-1. The examiner further stated that:

> *"Therefore, it would have been obvious to one of ordinary skill in the art at the time of applicant's invention to have provided the user configurable circuit (multiplexer 505) of Singh with the configurable memory circuit 232 and 234 as taught by Duong in order to provide configurable signal to control and program the multiplexer 505".*

The differences between prior art and current claims at issue in applying Graham v. Deere test is simply not that MUX 505 in FPGA 100 is user configurable; it pertains to the Applicant's conversion scheme "*a hard-wired circuit in lieu of said user configurable memory circuit*". The Examiner must show that crossbar 605 is a hard-wire circuit in lieu of configurable memory circuit (such as 232/234 as taught by Duong) in MUX 505. The Applicant respectfully submits that Duong teaching adds no value in this regard. Obviousness requires establishing that only a configurable memory circuit is hard-wired between an FPGA and an ASIC. Applicant believes that two basic requirements are not established: (i) logic circuit within MUX 505 exists exactly within ASIC 200, and (ii) logic circuit of MUX 505 within ASIC 200 is controlled by a hard-wired circuit in lieu of the user configurable memory circuit within FPGA 100. The examiner is also silent on (i) & (ii) in stating Graham v. Deere test. This is perhaps because logic circuits in MUX 505 are absent in Crossbar 605. Singh in view of Duong do not show NMOS in crossbar 605 of ASIC 200, nor show that pass-gates of ASIC 200 are controlled by hard-wire circuits. Singh in view of Duong do not disclose hard-wired configuration *memory* circuits at all.

As the Applicant detailed earlier, timing is significantly altered during Singh conversion. This is supported by the independent results in Appendix-2. As Singh conversion utilizes "configurable circuits" converted to "hard-wired circuits", it alters basic logic circuits within the device. Logic circuits carry timing critical signals. Configuration memory circuits do not carry timing signals. Schemes in which logic circuits alter lack the capacity to maintain substantially identical performance for the two fabricating options. Performance can be only maintained if "configurable memory circuits" can be altered without impacting a single "signal transient circuit path" within the entire die. The Applicant discloses such a technique.

(A4-2) Claim-3: On page-3 of the office action, in rejecting claim-3, the examiner stated that:

> "*Regarding claim 3, Singh in view of Duong discloses that wherein said second selectable option comprises a Read Only Memory (ROM) module (610 of Singh can be broadly interpreted as ROM)*".

The Applicant respectfully submits that one of ordinary skill in the art could not broadly interpret 610 structure of Singh as a ROM. It is a crossbar to connect one or more of 20 wires to a wire by inserting via(s) where needed. In the IC industry via's that connect metal lines to other metal lines are never called ROMs. In the ASIC industry this is normal interconnect procedure. The definition for ROM extracted from website "http://www.webopedia.com/TERM/R/ROM.html" is as follows:

> "*Pronounced rahm, acronym for read-only memory, computer memory on which data has been prerecorded. Once data has been written onto a ROM chip, it cannot be removed and can only be read.*
> *Unlike main memory (RAM), ROM retains its contents even when the computer is turned off. ROM is referred to as being nonvolatile, whereas RAM is volatile.*
> *Most personal computers contain a small amount of ROM that stores critical programs such as the program that boots the computer. In addition, ROMs are used extensively in calculators and peripheral devices such as laser printers, whose fonts are often stored in ROMs.*
> *A variation of a ROM is a PROM (programmable read-only memory). PROMs are manufactured as blank chips on which data can be written with a special device called a PROM programmer.*"

ROM mandates memory value storage. ROM coded interconnect is shown by the applicant in Fig-6 of the application and shown below as Dia-3 for convenience. Wire A is connected to B if the ROM value is "1", and wire A is disconnected from wire B if the ROM value is "0".

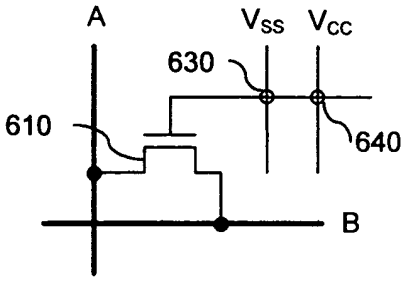


Fig-6

Dia-3

In a RAM/ROM based interconnect methodology; the memory element generates a control signal which is governed by the memory value, and the control signal governs connect/disconnect nature of the connection. In a via crossbar, the wires are simply connected or not connected as shown in Dia-2. No control signal is required to determine connect/disconnect nature of the connection. This is grounds to respectfully traverse the rejection, and to request withdrawal of the rejection.

(A4-3) Claim-8: On page-4 of the office action, in rejecting claim-8, the examiner stated that:

> *"Claims 8-13 and 16 are essentially the same as claims 1-7 as discussed above and are rejected similarly".*

In addition to arguments presented under (A4-1), the Applicant's claim-8 is specific to: logic circuits construction comprises one or more masking patterns that are invariant to the memory construction options. In rejecting claims 1-7 the examiner is silent to masking patterns or masks to construct FPGA 100 and ASIC 200. As the Applicant has described in detail, millions of geometries differ at transistor level between Singh FPGA 100 and ASIC 200, and no masking patterns or masks remain identical between the two devices. This is an added reason to traverse the rejection and to request withdrawal of the rejection.

(A4-4) Claim-17: On page-4 of the office action, in rejecting claim-17, the examiner stated that:

> *"Claims 8-13 and 16 are essentially the same as claims 1-7 as discussed above and are rejected similarly".*

In addition to arguments presented under (A4-1), the Applicant's claim-17 is specific to: a pass-gate configured by a memory element comprising a configurable RAM and hard-wire ROM

construction. Claim-17 further states that the pass-gate construction comprises one or more masking patterns that are invariant to the memory construction options. In rejecting claims-3, the examiner's assertion that Singh 610 can be broadly interpreted as a ROM structure is requested to be withdrawn. Duong in Fig-2 may show that in an FPGA, pass-gate logic is controlled by a configurable memory circuit, but this is of common knowledge. There is no demonstration by either Singh, or Duong, or Singh in view of Duong of an FPGA pass-gate logic controlled by the SRAM converted to an ASIC pass-gate logic controlled by hard-wire ROM. The examiner is silent to masking patterns or masks to construct MUX 505 and Crossbar 605. As the Applicant has described in detail, these are entirely different components, and no masking patterns or masks remain identical between the two constructions. Please note that all the pass-gate elements in MUX 505 shown as NMOS transistors in Dia-1 are absent in crossbar 605 construction shown in Dia-2. Withdrawal of the rejection is respectfully requested.

(A5) Prima Facie Obviousness:

(A5-1) Appearance of invention: A 103(a) rejection requires a prima facie obviousness of the prior art by Singh, in view of Duong. Furthermore:

> "*In order to support a holding of obviousness, a basic reference must be more than a design concept; it must have an appearance substantially the same as the claimed design. In re Harvey, 12 F.3d 1061, 29 USPQ2d 1206 (Fed. Cir. 1993). Absent such a reference, no holding of obviousness under 35 U.S.C. 103(a) can be made, whether based on a single reference alone or in view of modifications suggested by secondary prior art*".

Singh reference pertains to conventional design conversion from an FPGA to ASIC, and Duong reference only pertains to a specific programmable switch within an FPGA. In the Singh FPGA, since it is an FPGA, there may be a plurality of programmable elements such as the one presented by Duong as well as many others (those referenced by Applicant in the IDS disclosures). Singh in view of Duong adds no extra learning for FPGA to ASIC design conversion over that by Singh in itself. In the Singh conversion, a completely new ASIC device is constructed, similar to conventional design conversions. During the conversion, a soft-ware tool is utilized to extract and match timing between the FPGA and the ASIC by inserting delay elements into ASIC device. In the new ASIC device, even though LUT logic is matched, entirely new wire interconnects are provided. In the mechanics of the conversion, several millions of

transistors are removed while several millions of diodes & buffers are inserted. Duong provides no insight to ease this conversion.

In contrast, the Applicant specifies a simpler FPGA to ASIC conversion wherein the configuration memory circuit is simply hard-wired. The FPGA and ASIC have the same exact circuits, circuit layout, die size and pads. Only configuration memory circuit is altered between the two; in the FPGA it is a user configurable RAM and in the ASIC it is hard-wired ROM. No transistors are eliminated. No delay elements are inserted. The timing is transparently identical as no signal path is altered between the two devices. Prior art sighted by the examiner do not provide such device duality. Neither Singh nor Duong disclose: a first selectable fabrication option comprised of a user configurable memory circuit; and a second selectable fabrication option comprised of a hard-wired circuit in lieu of said user configurable memory circuit; wherein, the IC functionality and performance is substantially identical for a given configuration utilizing the first or second fabrication options. Withdrawal of the rejections is respectfully requested.

In Summary, the applicant believes that each of the independent claims (Claim 1, 8 & 17) are not obvious under Singh in view of Duong. It is clear to one familiar with prior art conventional design conversions that: (i) design conversions incur substituting configurable circuits by hard-wired circuits; (ii) substituting hard-wire circuits involve circuit modifications that alter signal transit delays, and (iii) masking patterns change during FPGA to ASIC conversions. Singh conversion also falls into conventional conversions. The Applicant has introduced a new device without these limitations. The applicant respectfully submits that the independent claims (1, 8, 17) and those dependent thereupon (claims 1-20) are not obvious by Singh in view of Duong. Withdrawal of the rejections to claims 1-20 is respectfully requested.

CONCLUSION

Applicant believes that the above discussion is fully responsive to all grounds of objections and rejections set forth in the Office Action.

If for any reason the Examiner believes that a telephone conference would in any way expedite prosecution of the subject application, the Examiner is invited to telephone the Inventor Mr. Madurawe at (408) 737-8868, or cell phone (408) 431-5367.

Respectfully submitted,

Raminda U. Madurawe

Applicant

Attachments:

Appendix-1: "Platform Flash ISP Configuration PROMs", Xilinx Inc., pp 1-4, DS 123 (v2.9) May 09, 2006.

Appendix-2: "Automated conversion from a LUT-based FPGA to LUT-based MPGA with fast turnaround time", Veredeas et al., pp 36-41, EDAA, 2006